WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising memory macro structures, and an access controller,

wherein each of said memory macro structures includes a plurality of memory banks having bank addresses allocated to said memory banks respectively, each of said memory banks containing a word line to be selected on the basis of a row address signal, a bit line to be selected on the basis of a column address signal so as to be connected to a data line of said memory macro structure, a memory cell provided at a point of intersection between said word line and said bit line, and a sense amplifier for latching storage information read out from said memory cell, and

wherein said access controller includes an address/command generating unit for operating for every memory bank, a hit/miss judgment unit for enabling data already latched by said sense amplifier to be output to said data line in response to an access request coming after data latching, and an address self-prefetching unit for self-prefetching an access address having a predetermined offset to an external access address after access control of said memory macro structure is effected with respect to said external access address so that data in said self-prefetched address is preread from said memory cells of said memory macro structure by said sense amplifier.

2. A semiconductor integrated circuit according

to Claim 1,

wherein said address signal output from said address/command generating unit is formed so that a bank address signal and a row address signal are mapped on a high order bit side of a column address signal and on a high order bit side of the bank address signal, respectively, and

wherein said predetermined offset is 2 to the power i from the least significant bit of said column address signal when i is the number of bits in said column address signal.

3. A semiconductor integrated circuit according to Claim 2, wherein said access address having said predetermined offset to said external access address is provided as an address for designating a memory bank different from a memory bank designated by said external access address.

4. A semiconductor integrated circuit according to Claim 3,

wherein said hit/miss judgment unit has a comparator for detecting coincidence/anticoincidence between said external access address and an access address for storage information held in said sense amplifier, and

wherein said address/command generating unit instructs said memory macro structure designated by said external access address to select a memory bank, a word line and a bit line in response to anticoincidence

detected by said comparator and instructs said memory macro structure designated by said external access address to suppress the word line selecting operation to select a memory bank and a bit line in response to coincidence detected by said comparator.

5. A semiconductor integrated circuit according to Claim 4,

wherein said hit/miss judgment unit further has an address register for registering information of said storage information access address held in said sense amplifier in accordance with every memory bank, and

wherein said comparator compares said access address information registered in said address register with a current access address and gives a result of the comparison to said address/command generating unit.

6. A semiconductor integrated circuit according to Claim 1, further

comprising a CPU connected to said access controller, and a first level cache memory connected to said CPU and said access controller,

said access controller including an address-alignment control unit for allocating an alignment contained in an address signal supplied from said CPU and different from an alignment of a plurality of address bits allocated to an index address of said first level cache memory to a bank address of said memory bank.

7. A semiconductor integrated circuit according to Claim 1, further comprising a CPU connected to said access controller, and a first level cache memory connected to said CPU and said access controller, said access controller being provided so that at least low order 2 bits of a tag address of said first level cache memory in an address signal supplied from said CPU are allocated to at least one of an address for designating said memory bank and an address for designating said memory macro structure.

8. A semiconductor integrated circuit according to Claim 1, further comprising a CPU connected to said access controller, and a first level cache memory connected both to said CPU and to said access controller, said access controller being provided so that at least low order 2 bits of an index address of said first level cache memory in an address signal supplied from said CPU are allocated to at least one of an address for designating said memory bank and an address for designating said memory macro structure.

9. A semiconductor integrated circuit according to Claim 1, further comprising a CPU connected to said access controller, and a first level cache memory connected to said CPU and said access controller, said access controller being provided so that at least low order 2 bits of an index address of said first level cache memory in an address signal supplied from said CPU are allocated to a column address signal.

10. A semiconductor integrated circuit according to Claim 4,

wherein said memory cells are dynamic memory cells, and

wherein commands supplied from said access controller contain a first command for instructing said memory macro structure to select said word line, and a second command for instructing said memory macro structure to select said bit line.

11. A data processing system comprising,

a CPU,

a first level cache memory connected to said CPU, and

a second level cache memory connected both to said first level cache memory and to said CPU and provided for said first level cache memory,

wherein said second level cache memory includes memory macro structures, and an access controller,

wherein each of said memory macro structures includes a plurality of memory banks having bank addresses allocated to said memory banks respectively, each of said memory banks containing a word line to be selected on the basis of a row address signal, a bit line to be selected on the basis of a column address signal so as to be connected to a data line of said memory macro structure, a memory cell provided at a point of intersection between said word line and said bit line, and a sense amplifier for latching storage

information read out from said memory cell, and

wherein said access controller has an address/command generating unit for operating for every memory bank, a hit/miss judgment unit for enabling data already latched by said sense amplifier to be output to said data line in response to an access request coming after data latching, and an address alignment control unit for changing bit alignment of an access address signal supplied from the outside of said access controller and supplying said access address signal with the changed bit alignment to said memory macro structure.

12. A data processing system according to Claim 11, wherein said address alignment control unit is provided so that an alignment contained in an address signal supplied from said CPU and different from the alignment of a plurality of address bits allocated to an index address of said first level cache memory is allocated to said bank addresses.

13. A data processing system according to Claim 11, wherein said address alignment control unit is provided so that at least a part of alignment of address information contained in an address signal supplied from said CPU and used as an index address of said first level cache memory is changed so as to be allocated to bank addresses of said memory banks.

14. A data processing system according to Claim 13, wherein said address alignment control unit is

provided so that a part of address information contained in an address signal supplied from said CPU and used as an index address of said first level cache memory and a part of address information contained in the address signal supplied from said CPU and used as a tag address are replaced with each other so as to be allocated to bank addresses of said memory banks.

15. A data processing system according to Claim 14, wherein said address alignment control unit has a switch circuit for making the alignment change of address information variable, and a control register for latching control information for determining a switch state of said switch circuit, said control register being enabled to be accessed by said CPU.

16. A data processing system according to Claim 11,

wherein said hit/miss judgment unit has a comparator for detecting coincidence/anticoincidence between an access address supplied from the outside and an access address of storage information held in said sense amplifier, and

wherein said address/command generating unit instructs said memory macro structure designated by an external access address to select a memory bank, a word line and a bit line in response to anticoincidence detected by said comparator while said address/command generating unit instructs said memory macro structure designated by an external access address to stop the

word line selecting operation and select a memory bank and a bit line in response to coincidence detected by said comparator.

17. A cache memory comprising DRAM macro structures, and an access controller,

wherein each of said DRAM macro structures includes a plurality of memory banks having bank addresses allocated thereto respectively, each of said memory banks containing a word line to be selected on the basis of a row address signal, a bit line to be selected on the basis of a column address signal so as to be connected to a data line of said DRAM macro structure, a memory cell provided at a point of intersection between said word line and said bit line, and a sense amplifier for latching storage information read out from said memory cell,

wherein said access controller includes an address/command generating unit for operating for every memory bank, and a hit/miss judgment unit for enabling data already latched by said sense amplifier to be output to said data line in response to an access request coming after data latching, and

wherein each of said memory banks has a first operation mode for activating said sense amplifier at first timing after selection of said word line, and a second operation mode for activating said sense amplifier at second timing later than said first timing after the selection of said word line.

18. A cache memory according to Claim 17, wherein said first operation mode is a write without data readout mode,

and

wherein said second operation mode is a refresh mode.

19. A cache memory according to Claim 17, wherein said cache memory is used in a data processing system having a first level cache memory connected to a CPU so that said cache memory is enabled to operate as a second level cache memory for said first level cache memory.

20. A semiconductor integrated circuit comprising an access controller including a first access port and a second access port, and a plurality of memory macro structures connected to said access controller through a data line peculiar to said access controller,

wherein each of said memory macro structures includes a plurality of memory banks having bank addresses allocated to said memory banks respectively, each of said memory banks containing a word line to be selected on the basis of a row address signal, a bit line to be selected on the basis of a column address signal so as to be connected to a data line of said memory macro structure, a memory cell provided at a point of intersection between said word line and said bit line, and a sense amplifier for latching storage information read out from said memory cells, and

wherein said access controller includes

selectors capable of selecting a memory macro structure to be accessed through said first access port and a memory macro structure to be accessed through said second access port respectively, an access priority judgment unit which permits parallel access through said first and second access ports when access through said first access port and access through said second access port use different memory macro structures, an address/command generating unit for operating for every memory bank with respect to said1 memory macro structure to be accessed, and a hit/miss judgment unit for enabling data already latched by said sense amplifier to be output to said data line in response to an access request coming after data latching.

21. A semiconductor integrated circuit according to Claim 20, wherein said access priority judgment unit gives priority to operation of one of the access ports having higher priority determined in advance when access through said first access port and access through said second access port use one and the same memory macro structure.

22. A semiconductor integrated circuit according to Claim 21, wherein at least one of said first and second access ports is provided with an SRAM interface function.

23. A semiconductor integrated circuit according to Claim 20, wherein, in a data processing system having a CPU, a first address bus, a first data bus, a bus

interface circuit, a second address bus, and a second data bus, said first access port is enabled to be connected to said CPU through said first address bus and said first data bus and said second access port is enabled to be connected to said bus interface circuit through said second address bus and said second data bus.

24. A semiconductor integrated circuit according to Claim 20,

wherein, in a data processing system having a CPU, a first level cache memory, a first address bus, a first data bus, a bus master, a second address bus, and a second data bus, said first access port is enabled to be connected to said CPU and said first level cache memory through said first address bus and said first data bus and said second access port is enabled to be connected to said bus master through said second address bus and said second data bus, and

wherein said semiconductor integrated circuit is enabled to operate as said second level cache memory for said first level cache memory.